EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	19243	(ddr or (double adj data adj rate))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:26
L2	865	(qdr or (quad adj data adj rate))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:26
L3	19842	1 or 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:26
L4	91	3 with pipelin$	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:27
L5	171391	(multiplexer or mux or mpx)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:27
L6	39	4 and 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:27
L7	4	("6011751", "6084802").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:28
L8	0	6 AND 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:28
L9	1	1 and 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:29

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L10	1	9 and 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:32
L11	0	10 and controller	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:34
L12	1	10 and fall$ and ris$	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:39
L13	48357	memory adj array	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:39
L14	0	12 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:40
L15	0	pipeline and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 18:59
L16	701	(710/7.ccls. or 710/20.ccls. or 710/21. ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 19:01
L17	0	16 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 19:01
L18	3031	711/104.ccls. or 711/105.ccls. or 711/157.ccls. or 711/167.ccls. or 711/167.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 19:02
L19	0	18 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 19:02

EAST Search History

L20	6328	365/189.02.ccls. or 365/189.05.ccls. or 365/233.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 19:03
L21	1	20 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 19:09
L22	501	thomann.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 19:09
L23	7	thomann-mark.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 19:10
L24	111	(double adj data adj rate adj memory).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 19:10
L25	0	((double adj data adj rate adj memory) with (first adj pipeline) with (second adj pipeline)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 19:11
L26	2	((double adj data adj rate adj memory) same (first adj pipeline) same (second adj pipeline)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/16 19:11

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1 Hybrid volume and polygon rendering with cube hardware
Kevin Kreeger, Arie Kaufman
July 1999 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**
Publisher: ACM Press
Full text available: pdf(1.85 MB) Additional Information: full citation, references, citings, index terms

Keywords: cube architecture, mixing polygons and volumes, ray casting, run-length-encoding, volume rendering

2 GPGPU: general purpose computation on graphics hardware
David Luebke, Mark Harris, Jens Krüger, Tim Purcell, Naga Govindaraju, Ian Buck, Cliff Woolley, Aaron Lefohn
August 2004 **Proceedings of the conference on SIGGRAPH 2004 course notes GRAPH '04**
Publisher: ACM Press
Full text available: pdf(63.03 MB) Additional Information: full citation, abstract

The graphics processor (GPU) on today's commodity video cards has evolved into an extremely powerful and flexible processor. The latest graphics architectures provide tremendous memory bandwidth and computational horsepower, with fully programmable vertex and pixel processing units that support vector operations up to full IEEE floating point precision. High level languages have emerged for graphics hardware, making this computational power accessible. Architecturally, GPUs are highly parallel s ...

3 Polygon rendering on a stream architecture
John D. Owens, William J. Dally, Ujval J. Kapasi, Scott Rixner, Peter Mattson, Ben Mowery
August 2000 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**
Publisher: ACM Press
Full text available: pdf(161.65 KB) Additional Information: full citation, abstract, references, citings, index terms

The use of a programmable stream architecture in polygon rendering provides a powerful mechanism to address the high performance needs of today's complex scenes as well as the need for flexibility and programmability in the polygon rendering pipeline. We describe

how a polygon rendering pipeline maps into data streams and kernels that operate on streams, and how this mapping is used to implement the polgyon rendering pipeline on Imagine, a programmable stream processor. We compare our resul ...

Keywords: OpenGL, SIMD, graphics hardware, kernels, media processors, polygon rendering, stream architecture, stream processing, streams

4 An overview of the BlueGene/L Supercomputer

NR Adiga, G Almasi, GS Almasi, Y Aridor, R Barik, D Beece, R Bellofatto, G Bhanot, R Bickford, M Blumrich, AA Bright, J Brunheroto, C Caşcaval, J Castaños, W Chan, L Ceze, P Coteus, S Chatterjee, D Chen, G Chiu, TM Cipolla, P Crumley, KM Desai, A Deutsch, T Domany, MB Dombrowa, W Donath, M Eleftheriou, C Erway, J Esch, B Fitch, J Gagliano, A Gara, R Garg, R Germain, ME Giampapa, B Gopalsamy, J Gunnels, M Gupta, F Gustavson, S Hall, RA Haring, D Heidel, P Heidelberger, LM Herger, D Hoenicke, RD Jackson, T Jamal-Eddine, GV Kopcsay, E Krevat, MP Kurhekar, AP Lanzetta, D Lieber, LK Liu, M Lu, M Mendell, A Misra, Y Moatti, L Mok, JE Moreira, BJ Nathanson, M Newton, M Ohmacht, A Oliner, V Pandit, RB Pudota, R Rand, R Regan, B Rubin, A Ruehli, S Rus, RK Sahoo, A Sanomiya, E Schenfeld, M Sharma, E Shmueli, S Singh, P Song, V Srinivasan, BD Steinmacher-Burow, K Strauss, C Surovic, R Swetz, T Takken, RB Tremaine, M Tsao, AR Umamaheshwaran, P Verma, P Vranas, TJC Ward, M Wazlowski, W Barrett, C Engel, B Drehmel, B Hilgart, D Hill, F Kasemkhani, D Krolak, CT Li, T Liebsch, J Marcella, A Muff, A Okomo, M Rouse, A Schram, M Tubbs, G Ulsh, C Wait, J Wittrup, M Bae, K Dockser, L Kissel, MK Seager, JS Vetter, K Yates
November 2002 **Proceedings of the 2002 ACM/IEEE conference on Supercomputing**

Publisher: IEEE Computer Society Press

Full text available: pdf(357.61 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper gives an overview of the BlueGene/L Supercomputer. This is a jointly funded research partnership between IBM and the Lawrence Livermore National Laboratory as part of the United States Department of Energy ASCI Advanced Architecture Research Program. Application performance and scaling studies have recently been initiated with partners at a number of academic and government institutions, including the San Diego Supercomputer Center and the California Institute of Technology. This mass ...

5 Single-Chip MPEG-2 422P@HL CODEC LSI with Multi-Chip Configuration for Large Scale Processing beyond HDTV Level

Hiroe Iwasaki, Jiro Naganuma, Koyo Nitta, Ken Nakamura, Takeshi Yoshitome, Mitsuo Ogura, Yasuyuki Nakajima, Yutaka Tashiro, Takayuki Onishi, Mitsuo Ikeda, Makoto Endo
March 2003 **Proceedings of the conference on Design, Automation and Test in Europe: Designers' Forum - Volume 2 DATE '03**

Publisher: IEEE Computer Society

Full text available: pdf(362.07 KB) Publisher Site Additional Information: full citation, abstract, index terms

This paper proposes a new architecture for VASA, a single-chip MPEG-2 422P@HL CODEC LSI with multi-chip configuration for large scale processing beyond the HDTV level, and demonstrates its flexibility and usefulness. This architecture consists of triple encoding cores, a decoding core, a multiplexer/de-multiplexer core, and several dedicated application-specific hardware modules with a hierarchical flexible communication scheme for high-performance data transfer. VASA is the worldýs first single ...

6 Session P9: interactive volume rendering: Texture hardware assisted rendering of time-varying volume data

Eric B. Lum, Kwan Liu Ma, John Clyne
October 2001 **Proceedings of the conference on Visualization '01**

Publisher: IEEE Computer Society
Full text available: pdf(11.72 MB) Additional Information: full citation, abstract, references, citings, index terms
Publisher Site

In this paper we present a hardware-assisted rendering technique coupled with a compression scheme for the interactive visual exploration of time-varying scalar volume data. A palette-based decoding technique and an adaptive bit allocation scheme are developed to fully utilize the texturing capability of a commodity 3-D graphics card. Using a single PC equipped with a modest amount of memory, a texture capable graphics card, and an inexpensive disk array, we are able to render hundreds of time s ...

Keywords: PC, compression, high performance computing, out-of-core processing, scientific visualization, texture hardware, time-varying data, transform encoding, volume rendering

7 GI-cube: an architecture for volumetric global illumination and rendering
Frank Dachille, Arie Kaufman
August 2000 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**
Publisher: ACM Press
Full text available: pdf(650.91 KB) Additional Information: full citation, abstract, references, citings, index terms

The power and utility of volume rendering is increased by global illumination. We present a hardware architecture, GI-Cube, designed to accelerate volume rendering, empower volumetric global illumination, and enable a host of ray-based volumetric processing. The algorithm reorders ray processing based on a partitioning of the volume. A cache enables efficient processing of coherent rays within a hardware pipeline. We study the flexibility and performance of this new architecture using both ...

Keywords: hardware accelerator, volume processing, volume rendering, volumetric global illumination, volumetric ray tracing

8 Embedded hardware design case studies: A fully-programmable memory management system optimizing queue handling at multi gigabit rates
G. Kornaros, I. Papaefstathiou, A. Nikologiannis, N. Zervos
June 2003 **Proceedings of the 40th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(236.13 KB) Additional Information: full citation, abstract, references, index terms

Two of the main bottlenecks when designing a network embedded system are very often the memory bandwidth and its capacity. This is mainly due to the extremely high speed of the state-of-the-art network links and to the fact that in order to support advanced quality of service (QoS), per-flow queueing is desirable. In this paper we describe the architecture of a memory manager that can provide up to 10Gbs of aggregate throughput while handling 512K queues. The presented system supports a complete ...

Keywords: memory management, network processor

9 Survey and taxonomy of packet classification techniques
David E. Taylor
September 2005 **ACM Computing Surveys (CSUR)**, Volume 37 Issue 3
Publisher: ACM Press

Full text available: pdf(1.60 MB) Additional Information: full citation, abstract, references, index terms

Packet classification is an enabling function for a variety of Internet applications including quality of service, security, monitoring, and multimedia communications. In order to classify a packet as belonging to a particular flow or set of flows, network nodes must perform a search over a set of filters using multiple fields of the packet as the search key. In general, there have been two major threads of research addressing packet classification, algorithmic and architectural. A few pioneerin ...

Keywords: Packet classification, flow identification

10 Queue Management in Network Processors

I. Papaefstathiou, T. Orphanoudakis, G. Kornaros, C. Kachris, I. Mavroidis, A. Nikologiannis

March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 3**

Publisher: IEEE Computer Society

Full text available: pdf(140.78 KB) Additional Information: full citation, abstract

One of the main bottlenecks when designing a network processing system is very often its memory subsystem. This is mainly due to the state-of-the-art network links operating at very high speeds and to the fact that in order to support advanced Quality of Service (QoS), a large number of independent queues is desirable. In this paper we analyze the performance bottlenecks of various data memory managers integrated in typical Network Processing Units (NPUs). We expose the performance limitations o ...

Keywords: Network processor, memory management, queue management

11 Research session: DB algorithms: Early hash join: a configurable algorithm for the efficient and early production of join results

Ramon Lawrence

August 2005 **Proceedings of the 31st international conference on Very large data bases VLDB '05**

Publisher: VLDB Endowment

Full text available: pdf(215.05 KB) Additional Information: full citation, abstract, references, index terms

Minimizing both the response time to produce the first few thousand results and the overall execution time is important for interactive querying. Current join algorithms either minimize the execution time at the expense of response time or minimize response time by producing results early without optimizing the total time. We present a hash-based join algorithm, called early hash join, which can be dynamically configured at any point during join processing to tradeoff faster production of result ...

12 Scalable high-speed prefix matching

Marcel Waldvogel, George Varghese, Jon Turner, Bernhard Plattner

November 2001 **ACM Transactions on Computer Systems (TOCS)**, Volume 19 Issue 4

Publisher: ACM Press

Full text available: pdf(933.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Finding the longest matching prefix from a database of keywords is an old problem with a number of applications, ranging from dictionary searches to advanced memory management to computational geometry. But perhaps today's most frequent best matching prefix lookups occur in the Internet, when forwarding packets from router to router. Internet traffic volume and link speeds are rapidly increasing; at the same time, a growing user population is increasing the size of routing tables against which p ...

Keywords: collision resolution, forwarding lookups, high-speed networking

13 Frequent value encoding for low power data buses

Jun Yang, Rajiv Gupta, Chuanjun Zhang
July 2004 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 9 Issue 3
Publisher: ACM Press
Full text available: pdf(1.79 MB) Additional Information: full citation, abstract, references, index terms

Since the I/O pins of a CPU are a significant source of energy consumption, work has been done on developing encoding schemes for reducing switching activity on external buses. Modest reductions in switching can be achieved for data and address buses using a number of general purpose encoding schemes. However, by exploiting the characteristic of memory reference locality, switching activity on the address bus can be reduced by as much as 66%. Till now no characteristic has been identified ...

Keywords: I/O pin capacitance, Low power data buses, encoding, internal capacitance, switching

14 Track 5: supercomputing (part1): ELDORADO

John Feo, David Harper, Simon Kahan, Petr Konecny
May 2005 **Proceedings of the 2nd conference on Computing frontiers**
Publisher: ACM Press
Full text available: pdf(374.11 KB) Additional Information: full citation, abstract, references, index terms

This paper introduces Eldorado, a third generation multithreaded architecture. Previous Cray multithreaded systems were plagued by unreliable hardware and high costs. Eldorado corrects these problems by using many parts built for other commercial systems. Its compute processor is a 500 MHZ multithreaded processor architecturally similar to the MTA-2 processor; but its interconnection network, I/O subsystem, and service processors are borrowed from other Cray systems. Eldorado retains the program ...

Keywords: heterogeneous architectures, multithreaded architectures, multithreaded processing, performance studies

15 Robust header compression (ROHC) in next-generation network processors

David E. Taylor, Andreas Herkersdorf, Andreas Döring, Gero Dittmann
August 2005 **IEEE/ACM Transactions on Networking (TON)**, Volume 13 Issue 4
Publisher: IEEE Press
Full text available: pdf(849.58 KB) Additional Information: full citation, abstract, references, index terms

Robust Header Compression (ROHC) provides for more efficient use of radio links for wireless communication in a packet switched network. Due to its potential advantages in the wireless access area and the proliferation of network processors in access infrastructure, there exists a need to understand the resource requirements and architectural implications of implementing ROHC in this environment. We present an analysis of the primary functional blocks of ROHC and extract the architectural implic ...

Keywords: ASIC, ASIP, FPGA, ROHC, hardware assist, header compression, network processor, reconfigurable hardware

16 Memory architecture for efficient utilization of SDRAM: a case study of the

computation/memory access trade-off
Thomas Gleerup, Hans Holten-Lund, Jan Madsen, Steen Pedersen
May 2000 **Proceedings of the eighth international workshop on Hardware/software codesign**
Publisher: ACM Press
Full text available: pdf(421.48 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper discusses the trade-off between calculations and memory accesses in a 3D graphics tile renderer for visualization of data from medical scanners. The performance requirement of this application is a frame rate of 25 frames per second when rendering 3D models with 2 million triangles, i.e. 50 million triangles per second, sustained (not peak). At present, a software implementation is capable of 3-4 frames per second for a 1 million triangle model.By usin ...

Keywords: 3D graphics, case study, memory architecture

17 Floorplanning: Floorplan assisted data rate enhancement through wire pipelining: a real assessment
Mario R. Casu, Luca Macchiarulo
April 2005 **Proceedings of the 2005 international symposium on physical design**
Publisher: ACM Press
Full text available: pdf(178.09 KB) Additional Information: full citation, abstract, references, index terms

The recent shift towards wire pipelining (WP) mandated by technological factors has attracted attention towards latency-controlled floorplanning. However, no systematic study has been published so far that takes into account block and logic delay limitations. The present workaims at filling the gap by showing that blockdelay can limit and possibly prevent any real gain WP might promise. Recurring to adaptive WP schemes, on the other hand, allows relevant gains. We built floorplanner that optimiz ...

Keywords: floorplanning, systems-on-chip, through-put, wire pipelining

18 The TM3270 Media-Processor
Jan-Willem van de Waerdt, Stamatis Vassiliadis, Sanjeev Das, Sebastian Mirolo, Chris Yen, Bill Zhong, Carlos Basto, Jean-Paul van Itegem, Dinesh Amirtharaj, Kulbhushan Kalra, Pedro Rodriguez, Hans van Antwerpen
November 2005 **Proceedings of the 38th annual IEEE/ACM International Symposium on Microarchitecture MICRO 38**
Publisher: IEEE Computer Society
Full text available: pdf(421.73 KB) Publisher Site Additional Information: full citation, abstract

We present the TM3270 media-processor, the latest TriMedia VLIW processor, tuned to address the performance demands of standard definition video processing, combined with embedded processor requirements for the consumer market. We discuss the architecture, implementation, and its first realization in a 90 nm process technology. The processor incorporates instruction set architectural (ISA) extensions and a load/store unit optimized for the video-processing domain. The ISA extensions improve the ...

19 Full papers: Tree bitmap: hardware/software IP lookups with incremental updates
Will Eatherton, George Varghese, Zubin Dittia
April 2004 **ACM SIGCOMM Computer Communication Review**, Volume 34 Issue 2
Publisher: ACM Press

Full text available: pdf(189.39 KB) Additional Information: full citation, abstract, references

Even with the significant focus on IP address lookup in the published literature as well as focus on this market by commercial semiconductor vendors, there is still a challenge for router architects to find solutions that simultaneously meet 3 criteria: scaling in terms of lookup speeds as well as table sizes, the ability to perform high speed updates, and the ability to fit into the overall memory architecture of an Level 3 forwarding engine or packet processor with low systems cost overhead. I ...

20 Design and Implementation of High-Performance Memory Systems for Future Packet Buffers

Jorge García, Jesús Corbal, Llorenç Cerdà, Mateo Valero

December 2003 **Proceedings of the 36th annual IEEE/ACM International Symposium on Microarchitecture**

Publisher: IEEE Computer Society

Full text available: pdf(348.55 KB) Additional Information: full citation, abstract, index terms

In this paper we address the design of a future high-speedrouter that supports line rates as high as OC-3072 (160 Gb/s),around one hundred ports and several service classes. Buildingsuch a high-speed router would raise many technological problems,one of them being the packet buffer design, mainly becausein router design it is important to provide worst-case bandwidthguarantees and not just average-case optimizations.A previous packet buffer design provides worst-case bandwidthguarantees by using ...

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IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1. **A 2.5-V, 333-Mb/s/pin, 1-Gbit, double-data-rate synchronous DRAM**
Hongil Yoon; Gi-Won Cha; Changsik Yoo; Nam-Jong Kim; Keum-Yong Kim; Cl Kyu-Nam Lim; Kyuchan Lee; Jun-Young Jeon; Tae Sung Jung; Hongsik Jeong Chung; Kinam Kim; Soo In Cho;
Solid-State Circuits, IEEE Journal of
Volume 34, Issue 11, Nov. 1999 Page(s):1589 - 1599
Digital Object Identifier 10.1109/4.799867
AbstractPlus | References | Full Text: PDF(688 KB) **IEEE JNL**
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2. **A 1.6-Gb/s/pin double data rate SDRAM with wave-pipelined CAS latency**
Sang-Bo Lee; Seong-Jin Jang; Jin-Seok Kwak; Sang-Jun Hwang; Young-Hyur Chil-Gee Lee;
Solid-State Circuits, IEEE Journal of
Volume 40, Issue 1, Jan. 2005 Page(s):223 - 232
Digital Object Identifier 10.1109/JSSC.2004.837983
AbstractPlus | Full Text: PDF(1496 KB) **IEEE JNL**
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3. **A high speed BIST architecture for DDR-SDRAM testing**
Sheng-Chih Shen; Hung-Ming Hsu; Yi-Wei Chang; Kuen-Jong Lee;
Memory Technology, Design, and Testing, 2005. MTDT 2005. 2005 IEEE Inter Workshop on
3-5 Aug. 2005 Page(s):52 - 57
Digital Object Identifier 10.1109/MTDT.2005.9
AbstractPlus | Full Text: PDF(184 KB) **IEEE CNF**
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4. **A 1 GHz power efficient single chip multiprocessor system for broadbanc applications**
Santhanam, S.; Allmon, R.; Anne, K.; Blake, R.; Bunger, N.; Campbell, B.; Carl Chen; Cheng, J.; Tuan Do; Dobberpuhl, D.; Ingino, J.; Kidd, D.; Kruckemyer, D Murray, D.; Nishimoto, S.; O'Donnell, L.; Oykher, M.; Panich, M.; Pearce, M.; F Rodriguez, D.; Rogenmoser, R.; Dongwook Suh; Sundaresan, V.; Supnet, E.; ' Yee, G.; Yiu, G.; Vo, C.; Wen, R.;
VLSI Circuits, 2001. Digest of Technical Papers. 2001 Symposium on
14-16 June 2001 Page(s):107 - 110
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